P1	Signal Assignment	P2
1/1A	CM REF	1/1A
2/2A	VIDEO 2-	2/2A
3/3A	VIDEO 2+	3/3A
4/4A	AUDIO 1-	4/4A
5/5A	AUDIO 1+	5/5A
6/6A	VIDEO 1-	6/6A
7/7A	VIDEO 1+	7/7A
8/8A	AUDIO 2-	8/8A
9/9A	AUDIO 2+	9/9A
10/10A	VIDEO 3-	10/10A
11/11A	VIDEO 3+	11/11A
12/12A	CL-	12/12A
13/13A	CL+	13/13A
14/1B	CM REF	14/1B
15/2B	AUDIO 3+	15/2B
16/3B	AUDIO 3-	16/3B
17/4B	VIDEO 4+	17/4B
18/5B	VIDEO 4-	18/5B
19/6B	AUDIO 4+	19/6B
20/7B	AUDIO 4-	20/7B
21/8B	X 1 +	21/8B
22/9B	X 1 -	22/9B
23/10B	X 2 +	23/20B
24/11B	X 2 -	24/11B
25/12B	X 3 +	25/12B
26/13B	X 3 -	26/13B

Figure 8. Contact and Signal Assignments for A/V/Control Cable Assemblies

5.3 Electrical Specifications

5.3.1 Cable Assembly Electrical Characteristics

An A/V/Control Cable Assembly shall meet the following set of electrical characteristics (as measured on a 2 meter long assembly).

Table 4
Cable Assembly Electrical Characteristics

Characteristic	Minimum	Maximum
Current Capacity	0.5 A per line	
Voltage Rating	250V AC rms.	
Dielectric Breakdown	500V AC rms. 1 minute, between adjacent contacts	
Insulation Resistance	500 M Ohms between adjacent contacts.	
DC resistance		0.55 Ohms
Differential Impedance measured by TDR.		100 Ohms
Mutual Capacitance, between wires of the same pair (measured differentially).		125 pico farads, total
Stray, pair-to-pair, Capacitance		15 pico farads, total
Attenuation: at 1 kHz at 1 MHz		 0.1 dB 0.1 dB
Crosstalk (near end and far end measure differential). at 1 MHz at 2 MHz at 4 MHz at 10 MHz		 -70 dB -65 dB -60 dB -55 dB
Resistance imbalance, between conductors of any pair		5 %

5.3.2 Termination

Termination of Audio pairs is not required.

Termination of Video pairs and reserved pairs shall be 120 Ω ± 2 %, 1/4 Watt minimum, non-inductive, at the first and last device attached to the Decoder Interface. Termination may be provided externally or, optionally, internally to the device by a selection mechanism.

5.4 Connectors

The A/V/Control cables and devices shall utilize a mating interface as specified in EIA 700 AOAD. The bus cables shall use male (plug) connectors on each end. Devices shall use female (header) connectors.

5.5 Audio Lines

Any supported audio lines shall meet the following requirements.

Table 5

Audio Input (Receiver)	
Input impedance (device on or off)	10 K Ohms differential, from DC to 100 kHz 5 K Ohms minimum from each line to +5.0 VDC
Input impedance matching (line-line)	90% minimum
Common Mode Range	5.0 V ± 2.0 V
Common Mode Rejection Ratio	60 dB minimum at 20 kHz

Table 6

Audio Output While Transmitting (Decoder)	
Output impedance	120 Ohms Differential, nominal 60 Ohms ±5% from each side to 5.0 VDC
Differential output voltage	2 V RMS ± 20%
Differential Gain Asymmetry	1% maximum DC - 20 kHz
Differential offset voltage	150 mV, maximum, when loaded as in Figure 9
Common mode voltage	5.0 ± 1.0 VDC

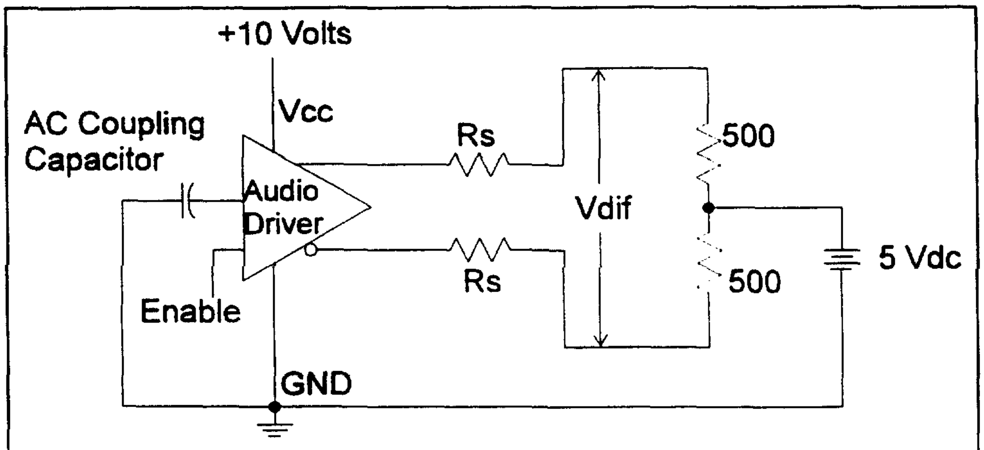


Figure 9. Audio Driver Test Circuit

Table 7

Audio Output Not Transmitting	
Output impedance (device on or off)	10 K Ohms Diff, minimum 5 K Ohms minimum from each line to +5.0 VDC
Impedance matching (line-line)	90% minimum
Differential output voltage	30 µVpp maximum into 1 K Ohm

A combined transmitter/receiver implementation shall maintain the 10 K Ohms minimum differential load impedance and impedance matching any time the device is not transmitting.

5.6 Video Lines

Video lines operate as a balanced differential 120 Ohm system. Termination of Video bus pairs shall be 120 Ohm, ±2%, 1/4 watt minimum, non inductive resistors, at the first and last device attached to the Decoder Interface. Termination may be provided externally or, optionally, internally to the device by a selection mechanism. Any supported video lines shall meet the following requirements.

Table 8

Video Input	
Input impedance (device on or off)	6 K Ohms Diff, from DC - 4 MHz 3 K Ohms, minimum from each line to +5.0 VDC
Input impedance matching (line-line)	90% minimum
Common Mode Range	5.0 V ± 2.0 V
Common Mode Rejection Ratio	35 dB minimum at 4 MHz

Table 9

Video Output While Transmitting	
Output impedance	120 Ohms Differential, nominal 60 Ohms ± 5% from each side to +5.0 VDC
Differential output voltage	
Composite video/luminance	1 Vpp ± 10% into 60 Ohm differential load
Chrominance (40 IRE burst)	286 mVpp ± 10% into 60 Ohm differential load
Differential Gain Symmetry	1% maximum at 4 MHz into 60 Ohm diff load
Differential offset voltage	50 mV, maximum, at 30 IRE, loaded as in Figure 10
Common mode voltage	5.0 ± 1.0 VDC

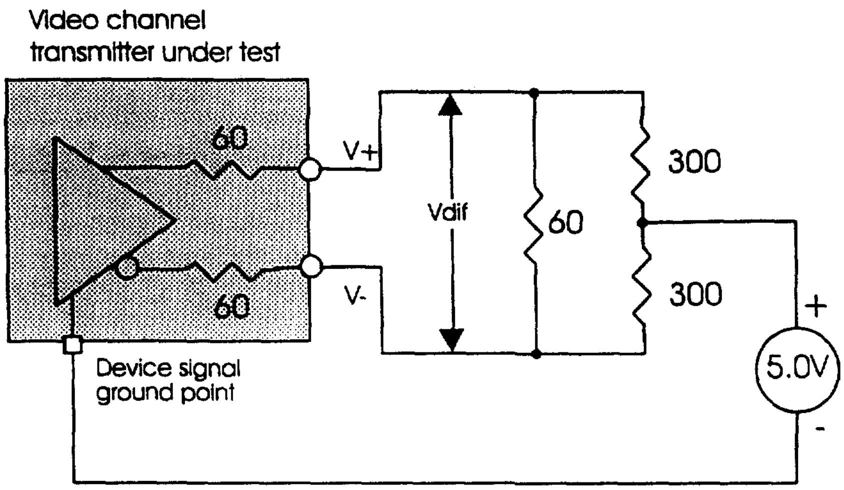


Figure 10. Video Driver Test Circuit

Table 10

Video Output Not Transmitting	
Output impedance	6 K Ohms differential, minimum, DC to 4 MHz 3 K Ohms minimum from each line to 5.0 VDC
Impedance matching (line-line)	90% minimum
Differential output voltage	1 mV_{pp} maximum into 120 Ohm

A combined transmitter/receiver implementation shall maintain the 3 K Ohms minimum differential load impedance and impedance matching any time the device is not transmitting.

5.7 Audio/Video Line Usage

Audio and Video lines on the A/V/Control connection are allocated according to the signal types to be transported. The capability of the Receiver or Decoder also dictates which A/V channels must be implemented.

5.7.1 Requirements Applying to Receiver

Table 11 indicates the hardware A/V lines that must be implemented in a television Receiver. A television Receiver with the capabilities shown in the left column is required to support audio and video lines of the A/V/Control connection as marked by an 'X' in the columns A1 to V4. Allocation of signals on these lines is defined in the companion document, IS-105.2

Table 11
A/V Channel Support Vs Television Receiver Capability

Television Receiver capability	A1	A2	A3	A4	V1	V2	V3	V4
Receiver mono	X							
Receiver stereo	X	X						
2 Tuner PIP, mono/none	X							
2 Tuner PIP, mono/mono	X		X					
2 Tuner PIP, stereo/none	X	X						
2 Tuner PIP, stereo/mono	X	X	X					
2 Tuner PIP, stereo/stereo	X	X	X	X				
Receiver Composite					X			
Receiver S-video					X	X		
2 Tuner PIP, comp/comp					X		X	
2 Tuner PIP, S-video/comp					X	X	X	
2 Tuner PIP, S-video/S-video					X	X	X	X

Similarly, table 12 shows the hardware A/V lines that must be implemented in a VCR Receiver.

Table 12
, **A/V Channel Support Vs VCR Receiver Capability**

VCR Receiver Capability	A1	A2	A3	A4	V1	V2	V3	V4
Mono VCR			X					
Stereo VCR			X	X				
Composite VCR							X	
S-video VCR							X	X

5.7.2 Requirements Applying to Decoder

Table 13 indicates the hardware A/V channels that must be implemented in a Decoder. A Decoder with the capabilities shown in the left column is required to support audio and video lines of the A/V/Control connection as marked by an 'X' in the columns A1 to V4. Allocation of signals on these channels is defined in the companion document, IS-105.2. Audio lines A1 and A2 may be used as a stereo pair, and audio lines A3 and A4 may be used as a stereo pair. If the Decoder produces monaural audio, the signal shall be placed on both lines of the pair. When a Decoder supplies monaural audio on both left and right, it must accomplish this without physically coupling the two audio busses together so that other Decoders do not suffer a loss of stereo separation.

Table 13
A/V Channel Support Vs Decoder Capability

Decoder capability	A1	A2	A3	A4	V1	V2	V3	V4
Decoder video only								
Decoder mono	X	X	X	X				
Decoder stereo	X	X	X	X				
Decoder Composite					X		X	
Decoder S-video					X	X	X	X

5.8 Common Mode Reference

The common mode reference contacts of each Decoder Interface device will be internally connected together and will connect to the device circuit signal ground through an internal series resistance of 200 Ohms. Figure 11 shows the Common Mode Reference connection.

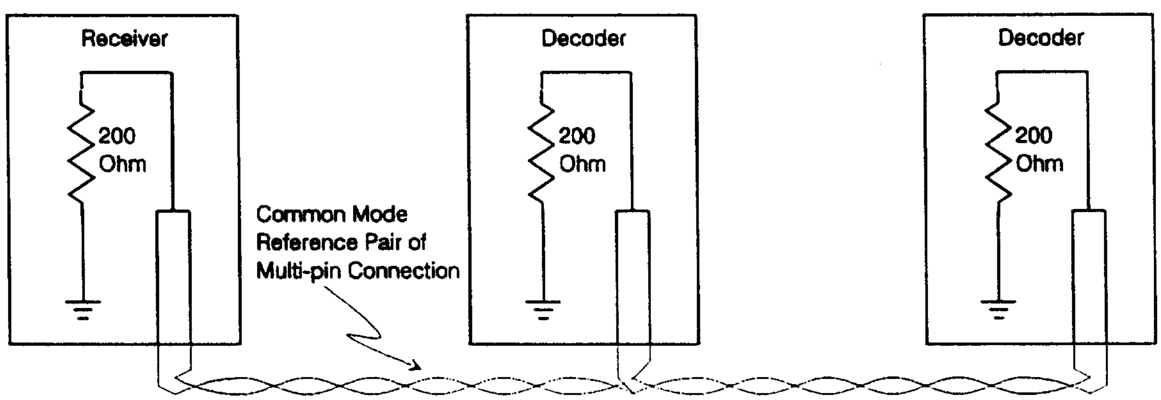


Figure 11. Common Mode Reference Connection

5.9 Control Line

5.9.1 Electrical and Encoding

This section defines the electrical specifications of the transceiver terminals that connect to the twisted pair via the "+" and "-" terminals.

Two electrical states are defined for the Control Line. These states are called Superior, in which a transmitter forces the medium, and Inferior, in which the transmitter is 'off' and may listen to the medium.

The Control Line employs two differential bipolar signal levels to represent the two media states of Superior and Inferior. Inferior state is represented by the presence of nominal -0.75V differential level present on the CL pair. The Superior state is represented by the presence of a nominal +0.75V differential level on the CL pair. These states are used to encode the symbols "1," "0," "EOF (End of Field)," and "EOP (End of Packet)."

The encoding of the symbols is strictly related to the time the Inferior or Superior state remains on the medium, not whether the Inferior or Superior state is used. Any symbol can be defined by either a Superior or Inferior state.

A Unit Symbol Time (UST) is defined to be 100 μs long. The "1" symbol is encoded as 1 UST without changing states. The "0" is defined to be two USTs, the "EOF" is three USTs, and the "EOP" is four USTs. Figure 12 shows an example of this encoding. The voltage levels shown are measured from the CL+ terminal with respect to the CL– terminal.

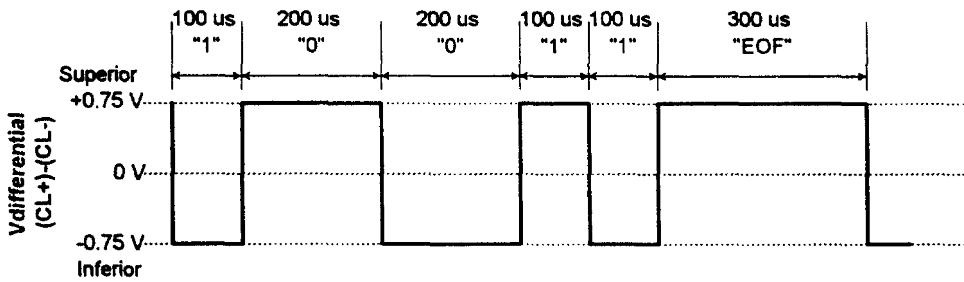


Figure 12. Symbol Encoding and Electrical Characteristics

5.9.2 Driver Output Specifications

Table 14

Superior State

Characteristic	Value
Output current into a short circuit from "+" to "-" terminals	10 ma +/- 25%
Output voltage with outputs open, from "-" to "+" terminals	+0.75 volt nominal, range = +0.5 volt to +1.0 volt
Common Mode Output voltage with "+" and "-" terminals shorted together and measured relative to transceiver circuit ground	Vcm = +5.0 ± 1.0 VDC
Common Mode Output Impedance with "+" and "-" terminals shorted together relative to transceiver circuit ground	Zcm(plus) = 469 Ohms +/- 25%
Common Mode Output Impedance with "+" and "-" terminals shorted together relative to transceiver positive supply	Zcm(minus) = 469 Ohms +/- 25%
Output Differential Balance: with "+" and "-" terminals tied together and tied to a +5.0 volt measurement supply (+/- 0.5% tolerance) with common of this supply grounded to transceiver circuit ground. Measure sum of currents from "+" and "-" terminals into +5.0 volt supply. This is "Icm".	Icm = +/- 1.2 ma maximum

Table 15

Inferior State

Characteristic	Value
Output current into a short circuit from "+" to "-" terminals	-0.33 ma +/- 25%
Output voltage with outputs open, from "-" to "+" terminals	-0.75 volt nominal, range = -0.5 volt to -1.0 volt
Common Mode Output voltage with "+" and "-" terminals shorted together and measured relative to transceiver circuit ground	Vcm = +5.0 ± 1.0 VDC
Common Mode Output Impedance with "+" and "-" terminals shorted together relative to transceiver circuit ground	Zcm (plus) = 15K Ohms +/- 25%
Common Mode Output Impedance with "+" and "-" terminals shorted together relative to transceiver positive supply	Zcm (minus) = 15K Ohms +/- 25%
Output Differential Balance: with "+" and "-" terminals tied together and tied to a +5.0 volt measurement supply (+/- 0.5% tolerance) with common of this supply grounded to transceiver circuit ground. Measure sum of currents from "+" and "-" terminals into +5.0 volt supply. This is "Icm".	Icm = +/- 60 µA maximum

5.9.3 Receiver Input Specifications

The following requirements define the electrical specifications of the transceiver receiver section that converts the twisted pair signals on the "+" and "-" terminals into the logic levels received by the device.

Receiver Threshold voltages

With a common mode voltage of 5.0 volts DC on the "+" and "-" terminals relative to the transceiver ground (Vcm) and with a test differential voltage applied from "-" to "+" (Vdif) the receiver shall have the following minimum characteristics:

Maximum Vdif required to detect superior state = +0.2 volt
Minimum Vdif required to detect inferior state = -0.2 volt

Receiver Common Mode Input range

The receiver shall meet the threshold voltage maximum and minimum when "Vcm," as defined above, is between +3 volts and +7 volts.

A reference schematic is provided in Figure 13 to clarify the Control Line electrical requirements. When Data In is low, the transmitter goes to the high impedance state, and the Control Line is in the Inferior state. Superior state is defined by a high input at Data In, which causes the transmit transistors to conduct. The differential Control Line voltage swings positive, and current is

supplied to any connected devices. Symbol detection is performed by a simple differential detector.
712 Figure 13 is illustrative only and not meant to define a standard implementation.

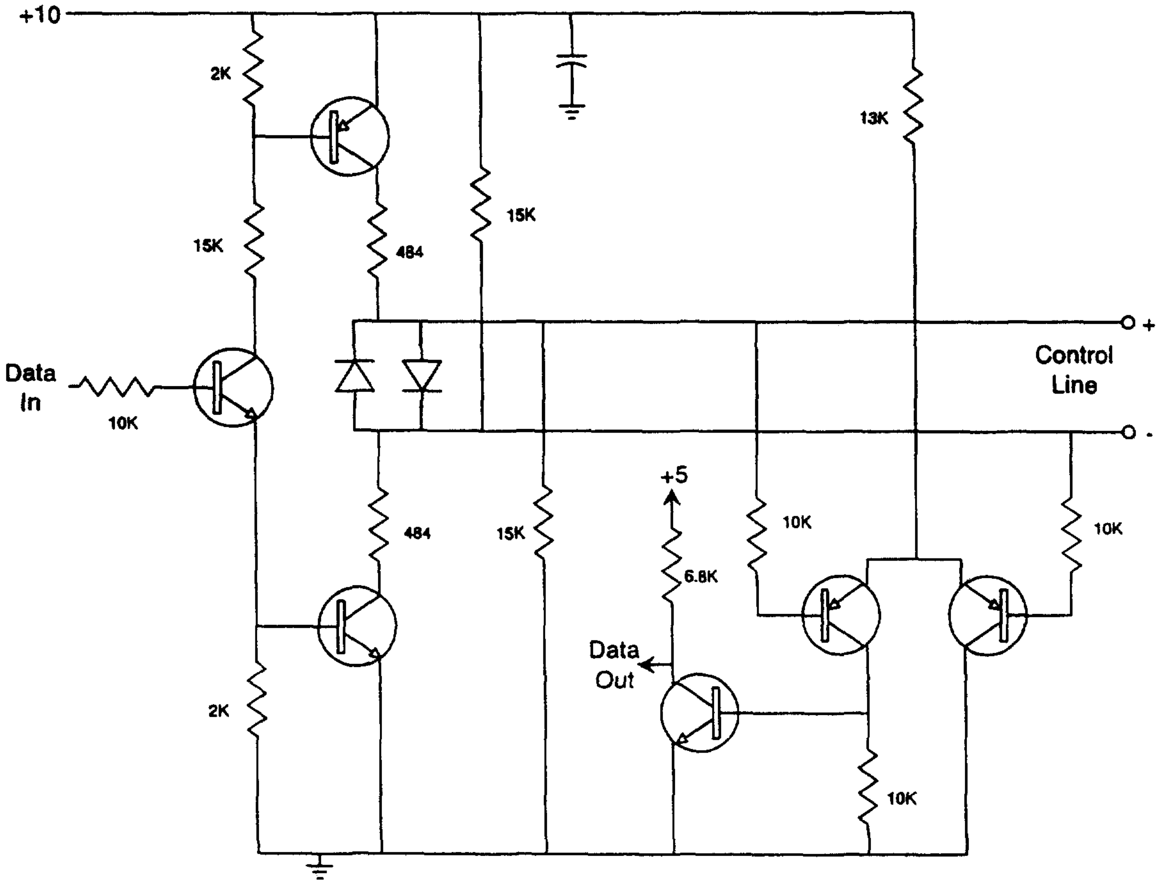


Figure 13. Example Control Line Transceiver

6. CHARACTERISTICS OF TRANSFER SWITCH

The transfer switch described in section 3.4 shall conform to the following parameters.

TABLE 16. SPECIFICATIONS APPLYING TO TRANSFER SWITCH

	ITEM	VALUE	TOLERANCE
1	Impedance	75 Ω	
2	Return Loss, 41-47 MHz	14 dB	Minimum
3	Frequency response, 41-47 MHz	±0.2 dB	peak to peak
4	Insertion loss, 41-47 MHz	≤0.7 dB	
5	Isolation, either input to output not selecting that input (unused input terminated)	70 dB	Minimum
6	d.c. resistance, input to output	5 Ω	Maximum when applied voltage is between 0 and 9.5 volts
7	Off resistance (input to non selected port	50 kΩ	Minimum
8	Leakage resistance to ground	100 kΩ	Minimum
9	Shunt capacitance to ground from any input	500 pF	Maximum

7. APPENDICES

7.1 A: Triple Beat Measurement

Figure 14 shows the test set-up for the measuring triple beat (TB) distortion product of the expander, as referenced in Table 3. Three CW oscillators, operating at frequencies as shown, are combined. Use of attenuators as shown is recommended in order to minimize interaction between oscillators. The combined output is set to a level of +30 dBmV per carrier, and supplied to the device under test (DUT). Verify that the input to the DUT is free of significant distortion. The amplitude of the TB distortion product appearing 0.5 MHz below the 46 MHz tone is measured with respect to the amplitude of the 46 MHz component. This is the required triple beat product.

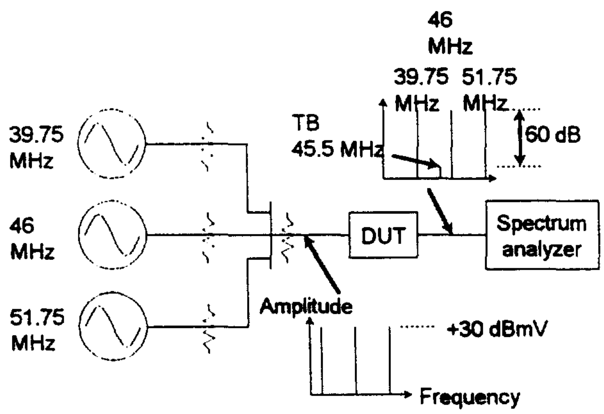


Figure 14. Triple Beat Measurement

7.2 B: Watch and Record Scenarios

This appendix illustrates ways in which various watch and record scenarios may be accomplished using the interface. The situations shown with one analog and one digital Decoder are illustrative only. Any combination of analog and digital Decoders may be used.

7.2.1 B1: Cable Ready TV and VCR with One Decoder Connected to TV

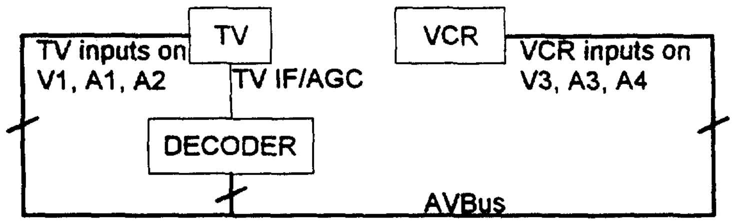


Figure 15. Cable Ready TV and VCR with One Decoder Connected to TV

(a.) Watch and record same scrambled channel:
Tune channel on TV tuner. Decoder outputs audio and video to TV on V1, A1 and A2, and to VCR on V3, A3 and A4.

(b) Watch and record two different unscrambled channels:
TV and VCR each use their internal IF; IF interface and AVBus not required.

(c) Watch a scrambled channel and record a clear channel:
Tune scrambled channel on TV tuner. Decoder receives IF input from TV; Audio and video from decoder to TV on V1, A1 and A2. VCR uses its internal IF, audio and video signals.

(d) Watch a clear channel and record a scrambled channel:
This case requires an IF switch (see figure 18).

7.2.2 B2: Cable Ready TV and VCR with One Decoder Connected to VCR

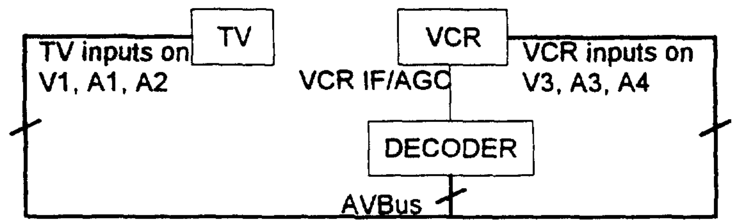


Figure 16. Cable Ready TV and VCR with One Decoder Connected to VCR

(a) Watch and record the same scrambled channel:
Tune channel on VCR tuner. Decoder outputs audio and video to TV on V1, A1 and A2; and to VCR on V3, A3 and A4.

(b) Watch and record two different unscrambled channels:
TV and VCR each use their internal IF; IF interface and AVBus not required.

(c) Watch a scrambled channel and record a clear channel:
This case requires an IF switch (see figure 18)

(d) Watch a clear channel and record a scrambled channel:
Tune scrambled channel on VCR tuner. Decoder receives IF input from VCR; Audio and video from decoder to VCR on V3, A3 and A4. TV uses its internal IF, audio and video signals.

7.2.3 B3: Cable Ready TV and VCR with Two Decoders

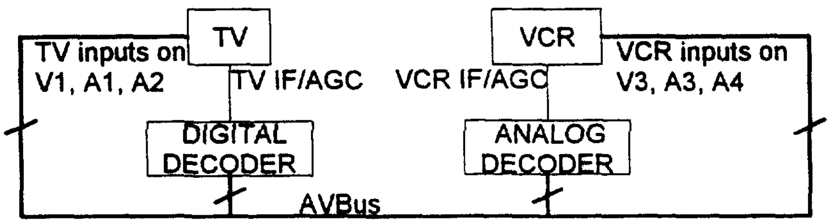


Figure 17. Cable Ready TV and VCR with Two Decoders

(a) Watch digital channel, record same digital
Digital Decoder receives IF from TV and outputs video and audio to TV on V1, A1 and A2; audio and video to VCR on V3, A3 and A4 (both TV and VCR are using the TV's tuner).

(b) Watch analog channel, record same analog channel:
Analog Decoder receives IF from VCR and outputs signals to TV and VCR as above (both TV and VCR are using VCR's tuner).

(c) Watch digital channel, record analog
Digital Decoder receives TV's IF and analog Decoder outputs audio and video to VCR on V3, A3 and A4 (TV using the TV's tuner and VCR is using the VCR's tuner).

(d) Watch analog channel, record digital
Analog Decoder receives VCR's IF and digital Decoder receives TV's IF. Audio and video to TV analog Decoder on V1, A1 and A2; audio and video from digital Decoder to VCR on V3, A3 and A4 (TV using VCR's tuner and VCR is using TV's tuner).

7.2.4 B4: Cable Ready TV and VCR with One Shared Decoder

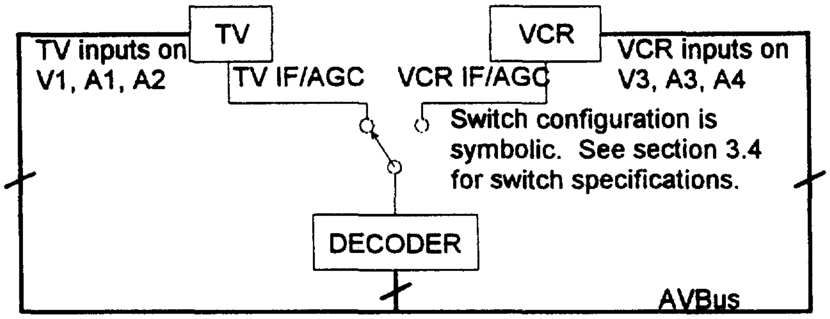


Figure 18. Cable Ready TV and VCR with One Shared Decoder

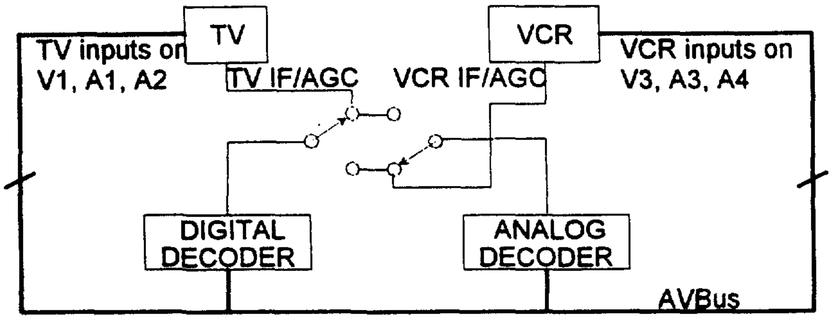
(a) Watch and record the same scrambled channel:
Tune channel on either TV or VCR tuner and switch decoder input to appropriate IF. Decoder outputs audio and video to TV on V1, A1 and A2, and to VCR on V3, A3 and A4.

(b) Watch and record two different unscrambled channels:
TV and VCR each use their internal IF; IF interface and AVBus not required.

(c) Watch a scrambled channel and record a clear channel:
Decoder receives IF input from TV; VCR uses its internal IF, audio and video signals. Audio and video from decoder to TV on V1, A1 and A2.

(d) Watch a clear channel and record a scrambled channel:
Decoder receives IF input from VCR and outputs audio and video to VCR on V3, A3 and A4. TV processing is all internal.

7.2.5 B5: Cable Ready TV and VCR with Two Shared Decoders



Switch configuration is symbolic. See section 3.4 for switch specifications.

Figure 19. Cable Ready TV and VCR with Two Shared Decoders

(a) Watch digital channel, record same digital channel:
Digital Decoder receives either TV or VCR IF and outputs video and audio to TV on V1, A1 and A2; Decoder outputs audio and video to VCR on V3, A3 and A4.

(b) Watch analog channel, record same analog channel:
As above but analog Decoder receives wither TV or VCR IF and outputs audio and video as above.

(c) Watch digital channel, record analog channel:
Digital Decoder receives TV IF and analog Decoder receives VCR IF. Digital Decoder outputs audio and video to TV on V1, A1 and A2. Analog Decoder outputs audio and video to VCR on V3, A3 and A4.

(d) Watch and record two different clear channels:
TV and VCR use internal Ifs and tune to required channels. No IF interface nor AVBus required.

7.3 C:' Loop Dynamics

This section includes information that should be useful in understanding the intended operation of the delayed AGC loop. In the mode in which the Decoder is controlling video demodulation, it must generate the delayed AGC signal used by the Receiver front end. This makes the dynamic performance of the AGC loop partially the domain of the Receiver, and partially the domain of the Decoder. In order for this to work, this document has attempted to outline a set of characteristics that should permit a stable loop under all conditions. This section provides background on how this is to be accomplished.

The primary pole in the delayed AGC closed loop response is R1-C1 (see figure 3). In order to have essentially the same pole location regardless of the source of control, resistor R1 must be high compared with R2, the pull-up resistor for the Receiver RF AGC. When the Decoder is not controlling AGC the output of amplifier A1 is at a high impedance (this may be accomplished by disabling the amplifier, or by a switch on the amplifier output). The signal from the Receiver may also drop close to zero volts, and this should not cause A1 to go to a low impedance state.

Figure 20 shows a typical delayed AGC curve, stated in terms of tuner gain vs. delayed AGC voltage. At high gain (low signal level) the voltage supplied by the Decoder will need to be nine volts plus or minus 0.5 volts to ensure the tuner is operating at maximum gain and lowest noise figure. As the signal increases the system moves to the left on the x-axis, lowering the gain. The gain vs. voltage curve becomes very non linear. Since this is a component in the loop gain of the delayed AGC, the loop dynamics are likely to vary considerably as a function of the gain reduction. This is not a problem so long as the designer takes the gain into account properly. As a guideline, the maximum slope is specified to be 25 dB/volt. The Decoder designer must ensure stability with this and all lower gains. Granted the loop dynamics will be particularly sloppy at some points, but this should not be a problem, as the signal level on the cable should not change rapidly.

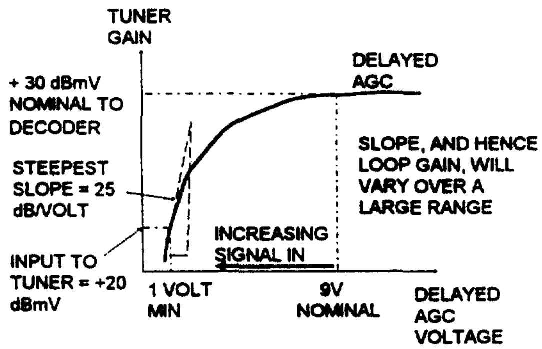


Figure 20. Delayed AGC Curve

In order to ensure that the delayed AGC threshold is placed where the tuner manufacturer intends, there must be a standardized IF level at the interface. This will allow the Decoder designer to accurately control the onset of delayed AGC control, while allowing the tuner manufacturer to set gain and AGC take-over (at the input) at a point deemed most suitable. Note however, that there is a tolerance to the maximum IF output level of the tuner, and the Decoder on-set of delayed gain control. If the Receiver's IF output is at the low end of the tolerance and the Decoder is at the high end of its tolerance, the tuner could be operating at 4 dB more output than intended, causing the third order distortion ratios (CTB, crossmodulation, etc.) to be 8 dB higher than expected.

Of concern too, is the need to ensure that the Decoder can effect a sufficiently wide gain control range. To so ensure, the specification includes the minimum delayed AGC voltage that should occur when the input to the Receiver is +20 dBmV. This permits the Decoder designer to know that the delayed AGC voltage can be controlled at the highest signal level anticipated. Nothing disastrous should happen if the signal level exceeds +20 dBmV, though the Decoder could loose gain control ability above this level, allowing the distortion characteristics of the tuner to increase to undesirable levels.

Figure 21 shows the operating range of the Receiver-Decoder system. At low input levels (toward the left in the figure) the tuner exhibits a certain gain, determined by the tuner manufacturer within limits. That minimum gain is +24 dB, measured from the Receiver's input to the IF output from the Receiver to the Decoder. The minimum gain value allows a reasonable noise figure for the Decoder, consistent with high carrier to noise ratio. In most practical cases the gain will be higher.

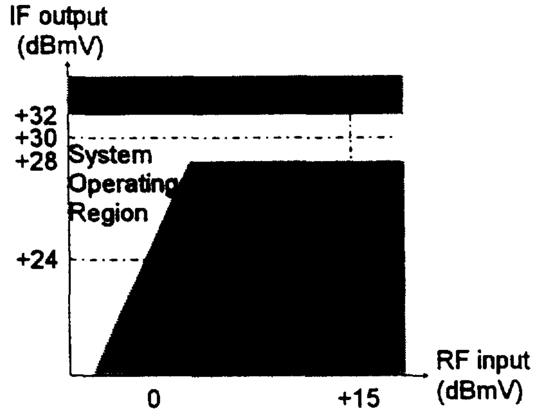


Figure 21. Nominal System Operating Levels

As the input level increases, the Receiver's IF output increases proportionally until the output is +30 dBmV, which is defined as the delayed AGC threshold. It is controlled in two parts: First, the Decoder manufacturer will hold the delayed AGC voltage high (+9 volts nominal) until the Receiver's IF output reaches +30 dBmV. At this point, the Decoder begins reducing the delayed AGC voltage to hold the Receiver's IF output constant. Next, the tuner manufacturer will determine the delayed AGC threshold for the tuner, by controlling the gain to the Decoder port.

Holding the Receiver's IF output constant for input levels exceeding the delayed AGC threshold is important to control distortion. In a cable environment the tuner may see signals on all possible channels from 54 MHz to 750 MHz, possibly increasing toward 1,000 MHz in the future.

7.4 D: Power Connector for Expander

7.4.1 D1. Expander Connector

The female connector (a.k.a. Right Angle Header) shown in Fig. 22 shall be used on the Expander, when a manufacturer chooses to equip the Expander to provide + 12 volt power to the Decoders.

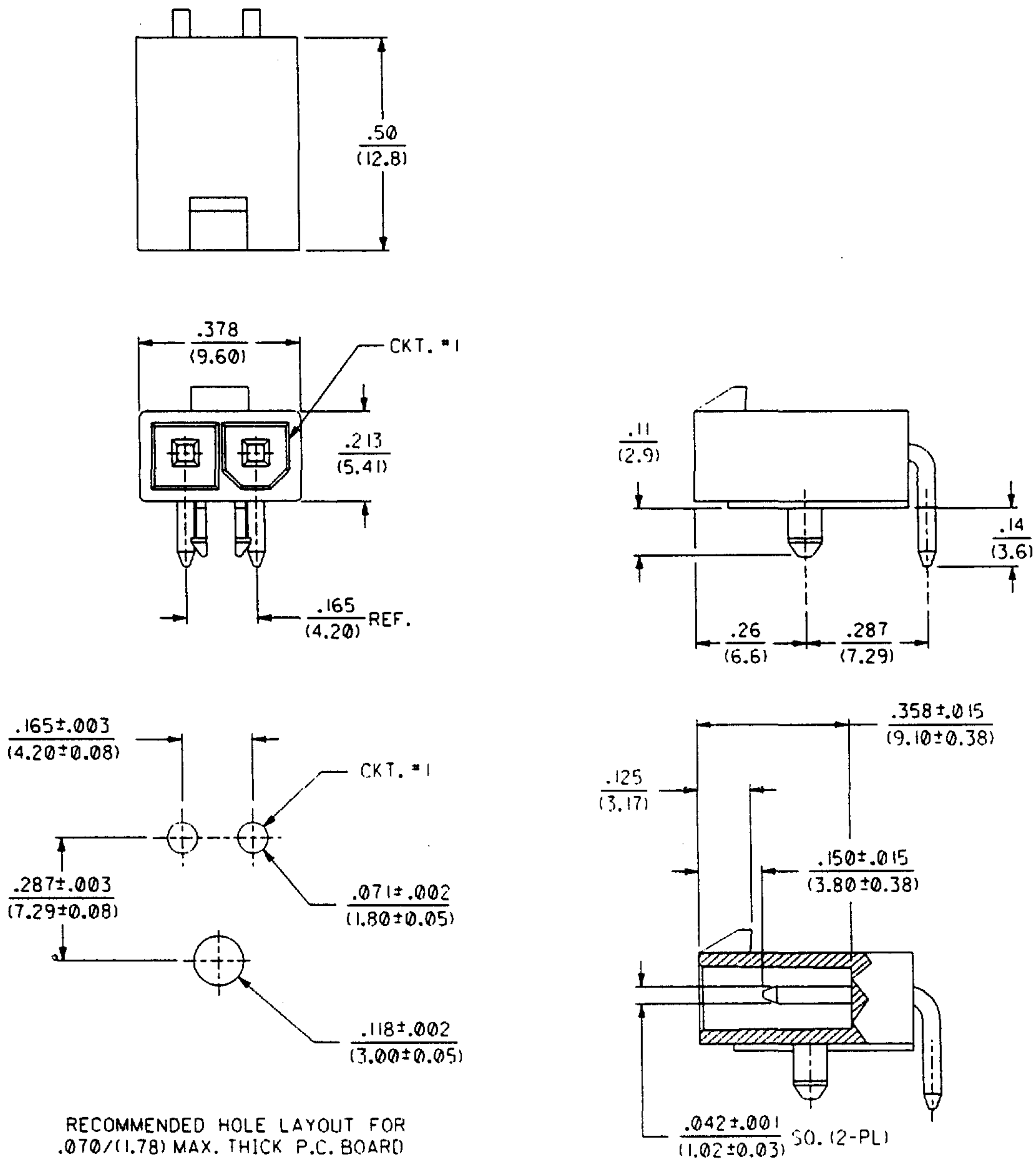


Figure 22. Connector for Use on Expander When a Manufacturer Chooses to Supply Power from the Expander to Decoders

Notes: 1. All dimensions shown in inches/(metric)
2. Tolerances ±.015/ ±(0.38) unless otherwise shown.
3. All drawings shown in third angle projection.

4. Pin material: Copper Alloy
5. Pin plating: .0002/(0.00508) min. Tin over .0001/(.0254) min. Copper.

7.4.2 D2. Decoder Connector

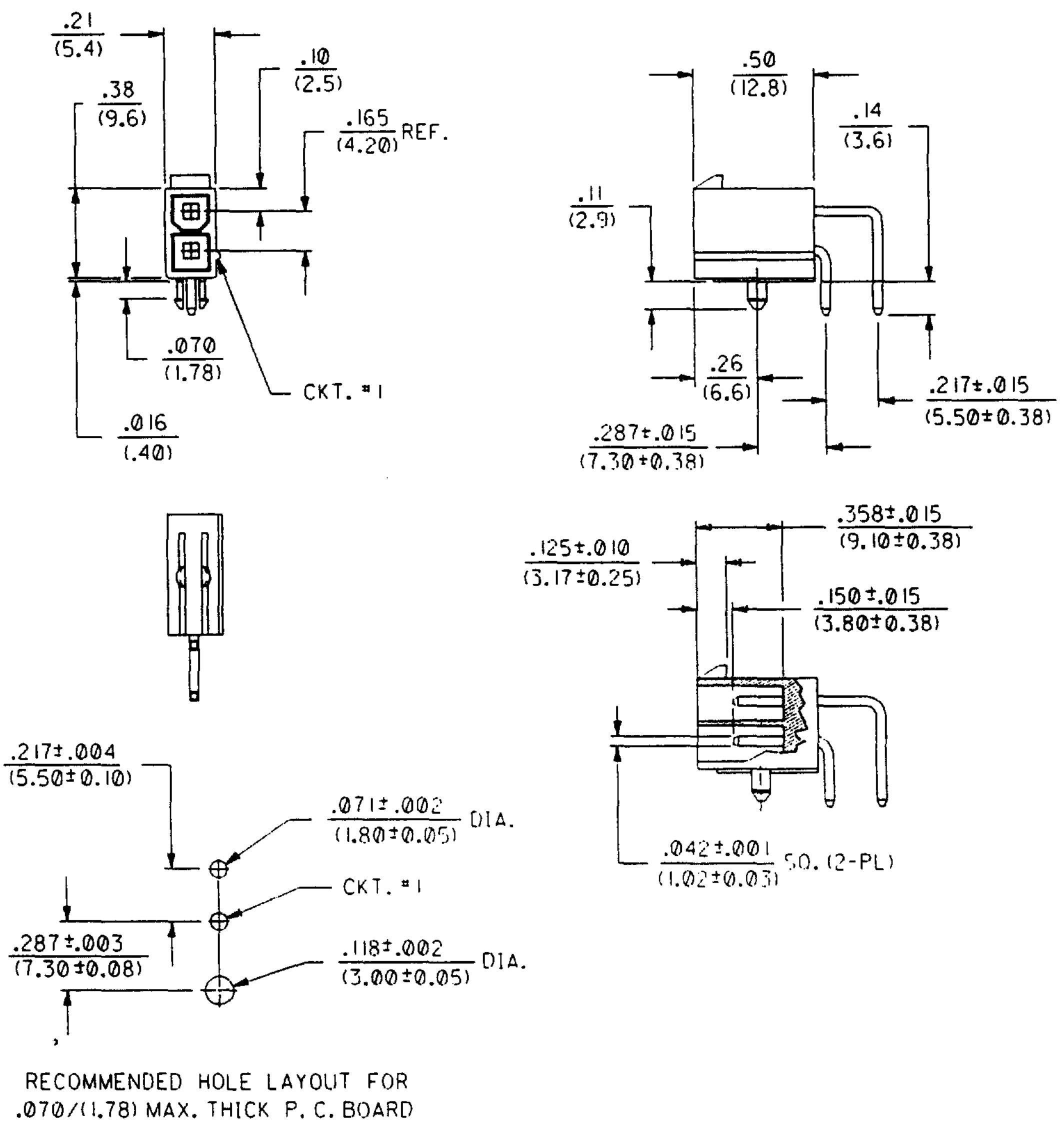


Figure 23. Connector for Use on Decoders Which Can Accept Power from the Expander

The female connector (a.k.a. Right Angle Header) shown in Fig. 23 shall be used on the Decoder, when a manufacturer chooses to equip the Decoder to receive its power from a power cable coming from the Expander.

Notes: 1. All dimensions shown in inches/(metric)
2. Tolerances ±.015/ ±(0.38) unless otherwise shown.

3. All drawings shown in third angle projection.
4. Pin material: Copper Alloy
5. Pin plating: .0002/(0.00508) min. Tin over .0001/(.0254) min. Copper.

7.4.3 D3. Male Cable Connector

The inter-mating dimensions of the Male Cable connector are shown here, as references only, to provide guidance for the construction of a cable assembly to provide power from an Expander to a Decoder. All of the information in Fig. 24 may be deviated from, provided that a Male Cable connector is configured to inter-mate and function properly when mated to the female connectors shown in Figs. 22 and 23.

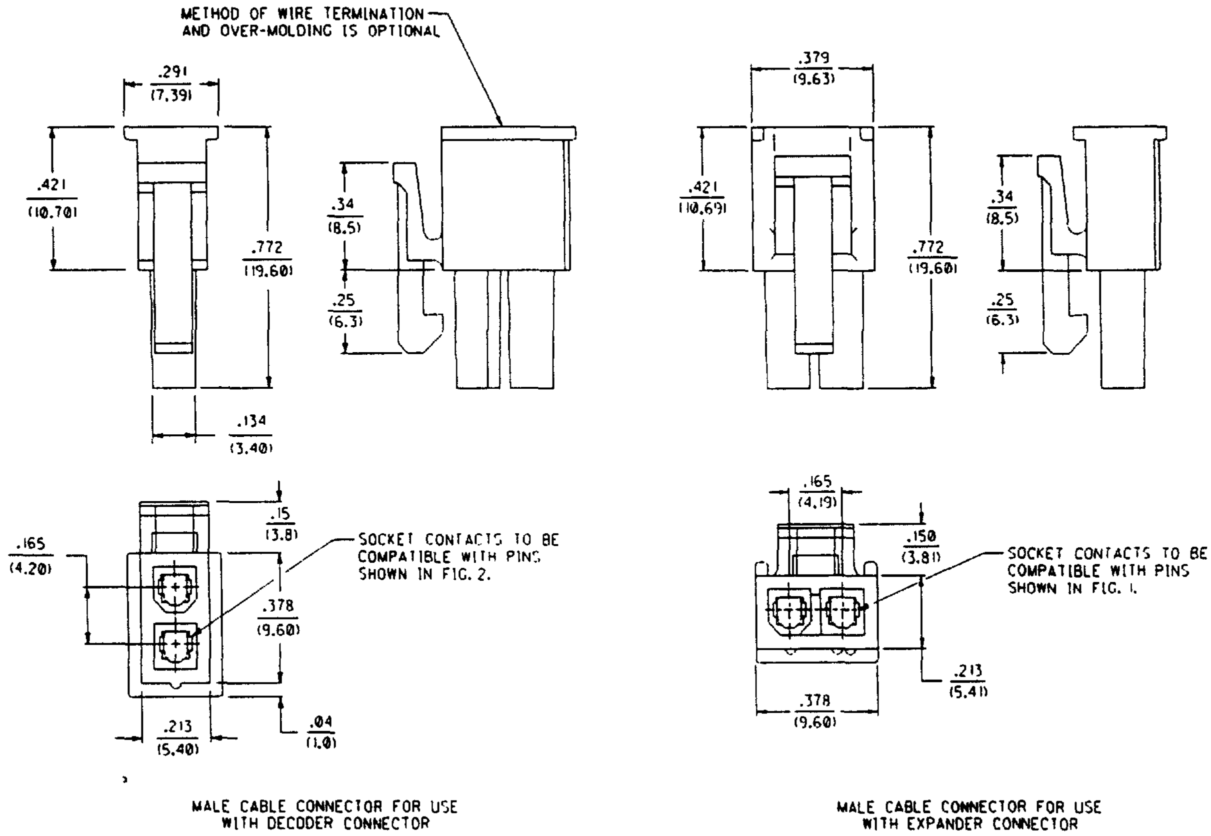


Figure 24. Suggested Connector for Use With Expander Power Cable

Notes: 1. All dimensions shown in inches/(metric)
2. Tolerances ±.015/ ±(0.38) unless otherwise shown.
3. All drawings shown in third angle projection.